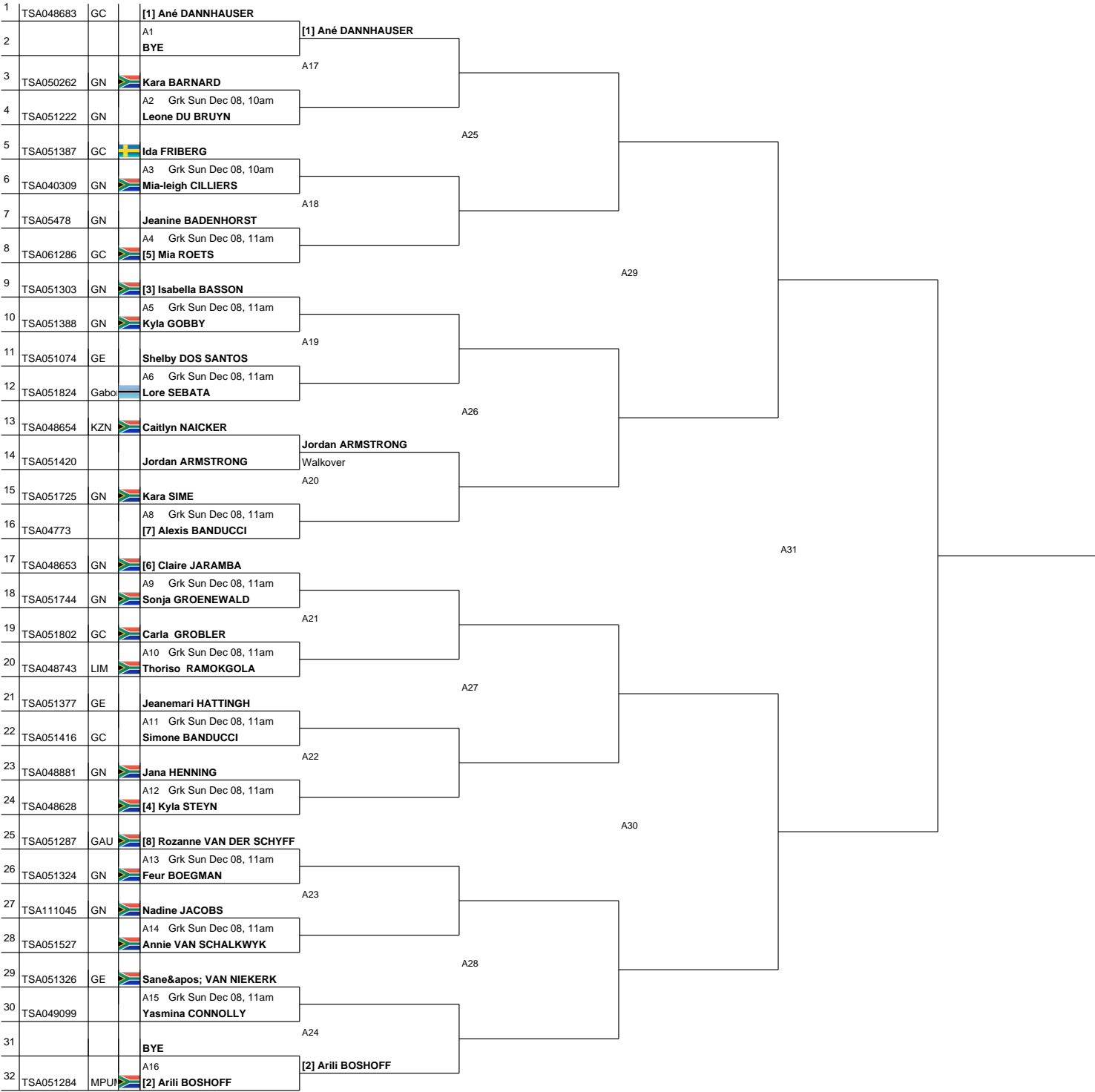


2019129 GN ProKennex Summer
GS 16

Main Draw

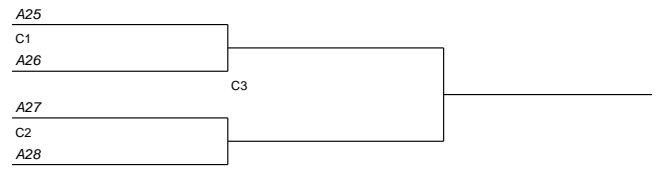


3/4 Playoff

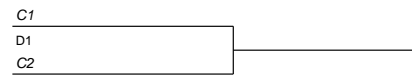
A29
B1
A30



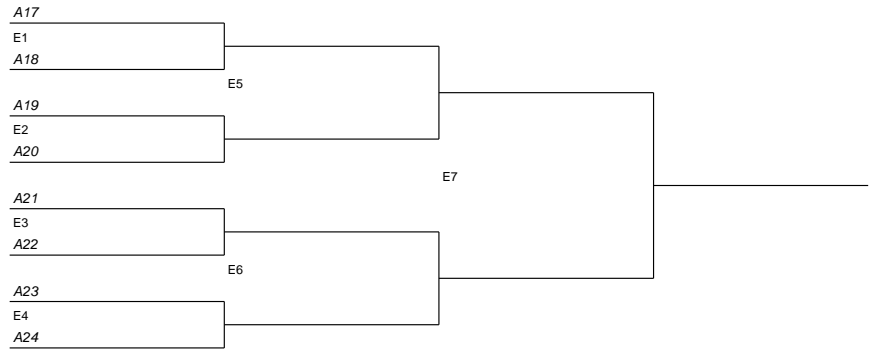
5/6 Playoff



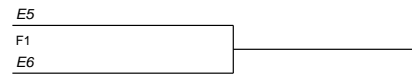
7/8 Playoff



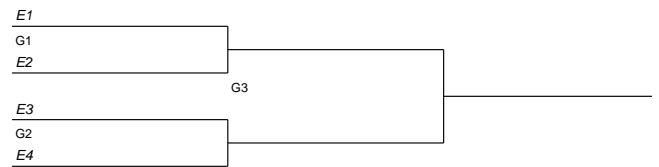
9/10 Playoff



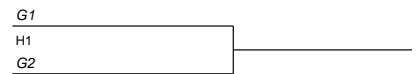
11/12 Playoff



13/14 Playoff



15/16 Playoff



The diagram illustrates a hierarchical tree structure for a 16-bit bus. The root node is labeled I15. It branches into two main sections. The left section contains nodes I13, I10, I11, and I14. The right section contains nodes I12 and I13. Each of these nodes further branches into specific data elements labeled I1 through I15, with some elements labeled 'A' (e.g., A1, A2, A3, A4, A5, A6, A8, A9, A10, A11, A12, A13, A14, A15) and others labeled 'BYE'.

```

graph LR
    I15 --- I13_L[I13]
    I15 --- I13_R[I13]
    I13_L --- I10
    I13_L --- I11
    I10 --- I1
    I10 --- I2
    I10 --- I3
    I10 --- I4
    I11 --- I5
    I11 --- I6
    I11 --- I7
    I11 --- I8
    I11 --- I9
    I14 --- I12
    I14 --- I13_R
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    I12 --- I
```

113

J1

114

The diagram shows a 3-to-1 multiplexer. It has four data inputs labeled I_9 , I_{10} , I_{11} , and I_{12} . There are three select lines labeled K_1 , K_2 , and K_3 . The inputs I_9 and I_{10} are connected to the top input of the multiplexer, while I_{11} and I_{12} are connected to the bottom input. The select lines K_1 and K_2 are connected to the select input of the multiplexer, and K_3 is connected to the enable input. The output of the multiplexer is a single line on the right.

K1	
L1	
K2	

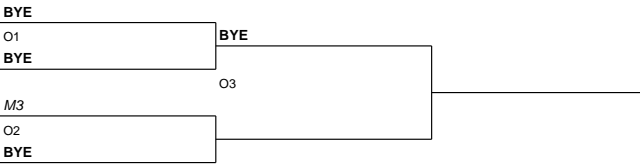
Diagram illustrating a 4-stage merge sort algorithm:

- Stage 1:** Initial data segments: `BYE | M1 | /2` and `M2 | BYE`.
- Stage 2:** First merge: `/3 | M2 | BYE` (labeled M5) and `/5 | M3 | /6` (labeled M6).
- Stage 3:** Second merge: `/7 | M4 | BYE` (labeled M6) and `M7`.
- Stage 4:** Final merge: `M7`.

M5	
N1	
M6	



29/30 Playoff



31/32 Playoff

